REMARKS

Original claims 1-4 were filed in the above-identified application with claims 1 and 4 being independent. In response to a Restriction Requirement, claims 1, 2 and 4 were elected. With this Amendment, claims 1 and 4 are being amended, claims 5-16 are being added with claims 13 and 15 being independent and claim 2 is being cancelled. Accordingly, claims 1, 2, 4-16 are at issue in the above-identified application with claims 1, 4, 13 and 15 being independent.

Rejection under 35 U.S.C. §102

Claims 1-2 and 4 were rejected under 35 U.S.C. § 102(e) as being allegedly unpatentable over *Yamamoto* (U.S. Patent No. 6,413,833). Applicants respectfully traverse this rejection. Claims 1 and 3 were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by *Watanabe et al.* (1992). Applicants respectfully traverse this rejection. Claim 3 is not at issue since claims 1, 2 and 4 were elected in an earlier Restriction Requirement. Claims 1 and 4 have been amended to further define the method of forming a capacitor. As now amended, the present invention claims that the bottom electrode is etched using an aqueous solution containing potassium hydroxide.

The Applicants respectfully note that the cited references do not fairly teach or suggest this etching. Therefore, the references do not anticipate the present invention.

Rejection Under 35 U.S.C. 103(a)

Claims 2 and 4 were rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over *Watanabe et al.* Applicants respectfully traverse this rejection.

The present invention teaches etching the bottom layer using an aqueous solution containing potassium hydroxide or using an organic alkaline aqueous solution such as a hydroxylamine aqueous solution. In contrast, the cited references only disclose NH_3-H_2O_2-H_2O; HF-H_2O_2-H_2O; HF-HNO_3-H_2O and HF-H_2O.

By using an aqueous solution containing potassium hydroxide or using an organic alkaline aqueous solution such as a hydroxylamine aqueous solution, the present invention removes the natural oxide film and contamination on the bottom substrate. Thus, any organic substance is removed by the etching. Accordingly, the exposed amorphous silicon surface of the bottom electrode is free from contamination (see specification page 15, lines 1-2). Thus, the HSG-Si 19 grows on the entire surface of the bottom electrode to increase the capacitance of the capacitor (see specification page 15, lines 3-10).

Additionally, the present invention teaches an etching stopping layer which assists in forming better HSG capacitance by preventing voids in the inter-layer insulating film (see specification page 12, lines 10-12).

To establish a prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art See In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Further, not only must the Examiner find each element of the claimed invention in the prior art, the Examiner must show upon "rigorous application" the proper motivation or suggestion to combine wherein the showing "must be clear and particular" See In re Dembiczak, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 17 (Fed. Cir. 1999).

In order to meet an obviousness requirement, the requirement has to meet some suggestion that the cited references have similar features or structures. To suggest otherwise

pertains to an impermissible hindsight reconstruction. The standard, rather, is whether the reference taken as a whole would have suggested the applicant's invention to one of ordinary skill in the plasma display arts at the time the invention was made.

II. Conclusion

In view of the above amendments and remarks, Applicants submit that all claims are clearly allowable over the cited prior art, and respectfully request early and favorable notification to that effect.

Respectfully submitted,

Dated: April 17, 2003 By: Brian J. Gill

Brian J. Gill
Registration No. 46,727
SONNENSCHEIN NATH & ROSENTHAL
P.O. Box 061080
Wacker Drive Station, Sears Tower
Chicago, Illinois 60606-1080
(312) 876-8000

APPENDIX A
VERSION WITH MARKINGS TO SHOW CHANGES

In The Specification

Please substitute the paragraph beginning on page 1, line 2 with the following paragraph:

To increase the capacitance [the more], Japanese Published Unexamined Patent Application No. Hei 8-306646 proposes a method in which hemispherical grained silicon (referred to as HSG-Si hereinafter) is formed on the surface of an electrode.

Please substitute the last paragraph on page 3 with the following paragraph:

In detail, organic substance that is generated during the process is deposited on the surface of the core pattern 2a formed on the cylinder core layer 2 described with reference to FIG. 3A. Such organic substance is taken into the core [pattern2a], pattern 2a side surface layer of the amorphous silicon film 3 formed so as to cover the inside wall of the core pattern 2a. A natural oxide layer that has grown on the surfact of the bottom electrode 3a is removed by means of etching of the bottom electrode 3a with diluted hydrofluoric acid, but amorphous silicon that is the component of the bottom electrode 3a and organic substance can not be removed by means of etching with diluted hydrofluoric acid. As a result, the surface layer of the bottom electrode 3a where organic substance has been taken in remains.

Please substitute the first paragraph on page 9 with the following paragraph:

Next, the inter-layer insulating film 13 is subjected to anisotropic etching with aid of a resist patter used as a mask not show in the drawing to thereby form a contact hole 14 that extends to the semiconductor substrate 11 on the inter-layer insulating film 13. Herein, a

diffusion layer formed on the semiconductor substrate 11 just under the contact hole is not shown in the drawing. Then, the resist pattern is removed, and a conductive layer is embedded in the internal of the contact hole 14 to obtain a contact electrode 15 that is connected to the semiconductor substrate 11. Next, an etching stopper layer 16 is formed on the inter-layer insulating film 13 and the contact electrode [14] 15. The etching stopper layer 16 is a layer having a film thickness of, for example, 100 nm consisting of silicon nitride to be served as a stopper layer when a cylinder core layer is removed later.

Please substitute the paragraph beginning on page 11, line 12 with the following paragraph:

The amorphous silicon film 18 disposed on the cylinder core layer 17 is removed by means of CMP process in the above-mentioned case, otherwise a method, in which a silicon oxide film (for example, NSG) is formed [is formed] on the amorphous silicon film 18 at a temperature that is not favorable for crystallization of amorphous silicon[, the]. The silicon oxide film and amorphous silicon film 18 are removed by means of isotropic RIE (reactive ion etching) process from the surface side of the silicon oxide film to thereby remove partially the amorphous silicon film 18 excepting the amorphous silicon film 18 that covers the inside wall of the core pattern 17a[, may be applied].

Please substitute the paragraph beginning on page 21, line 14 with the following paragraph:

Thereafter, as shown in [FIG.] FIG. 2G, a natural oxide film (not shown in the drawing) generated on the surface layer of the bottom electrode 39a and the exposed amorphous silicon surface layer that is the component of the bottom electrode 39a are removed by means of etching. Herein, the natural oxide layer (not shown in the drawing) and the exposed amorphous silicon surface layer that is the component of the bottom electrode 39a are removed by means of etching with a strong alkaline aqueous solution etchant. The wet etching is carried out in the same manner as used in the first embodiment described with referenced to FIGF.1F.

In The Claims

1. (Amended) A method for forming a capacitor comprising:

a first step for forming an amorphous silicon film so as to cover hole-type or island-type core pattern formed on a substrate,

a second step for removing said amorphous silicon film so that said amorphous silicon film remains on the side wall of said core pattern to thereby form a cylindrical bottom electrode having the peripheral wall that is said amorphous silicon film remaining on the side wall of said core pattern,

a third step for removing said core pattern by means of etching,

a fourth step for removing the natural oxide film formed on the surface of said bottom electrode and the amorphous silicon surface layer that is the component of said bottom electrode by means of etching using an aqueous solution containing potassium hydroxide, and

a fifth step for forming semispherical silicon grains on the surface of said bottom electrode.

4. (Amended) A method for forming a capacitor comprising:

a first step for forming an amorphous silicon film so as to cover hole-type or island-type core pattern formed on a substrate.

a second step for removing said amorphous silicon film so that said amorphous silicon film remains on side wall of said core pattern to thereby form a cylindrical bottom electrode having the peripheral wall that is the said amorphous silicon film remaining on the side wall of said core pattern.

a third step for removing said core pattern by means of etching,

a fourth step for removing the surface layer of said bottom electrode by use of an [aqueous mixture solution containing nitric acid and hydrofluoric acid] <u>aqueous solution containing potassium hydroxide</u>, and

a fifth step for forming semispherical silicon grains on the surface of said bottom electrode.